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10/685,496	10/16/2003	Chih-Jen Huang	025796-00010	5365

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EXAMINER	
YOHA, CONNIE C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H'A

Office Action Summary	**Application No.** 10/685,496	**Applicant(s)** HUANG, CHIH-JEN	
	Examiner Connie C. Yoha	**Art Unit** 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The Amendment filed on 6/15/05 has been entered and are made of record.

2. Claims 1, and 3-10 are amended.

3. Claims 2 and 11 are canceled.

4. Claims 1, 3-10 are pending.

5. Claim 1, and 3-10 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Onakado et al, Pat. No. 5818761.

The reason for this rejection has been set forth in the previous action.

Response to Arguments

6 Applicant's argument filed 6/15/05 has been fully considered.

Drawing objection, claim rejection-35 USC 112 are now withdrawn.

However, claim rejection-35 USC 112 first paragraph to claim 9 is still stands (see 35 USC 112 first paragraph rejection below).

Previously, Applicant's arguments with respect to claims 5-10 have been considered but are moot in view of the new ground(s) of rejection due to the amended claims. Examiner uses new cited reference (Lin et al, U.S. Pat. 6671209) to reject claim 5-10 in addition to the original rejection set forth in the previous office action.

7. Applicant's arguments filed 6/15/05 have been fully considered but they are not persuasive.

In response to the applicant's argument concerning the amended claims 1, 5 and 10 in that Onakado et al '761 discloses applying an **erase voltage to the P-type source** (of about +5 to +12 V) and N-type well region and **floating the P-type drain**, of which is not as claimed in the instant application. The instant application claimed, "applying **an erase voltage to the P-type drain region**, and to the N-type well region and **floating the P-type source region".** Examiner agreed with the applicant with such statement, however, as stated in the previous office action, examiner had explained that, in the semiconductor memory device, it is inherently known that a drain and a source can be used interchangeably within a memory device without affecting or inducing the different operating result (especially since the claimed source and drain are of the same type of conductivity (P-type) of which the operation of the source and the drain are the same, therefore, the source and drain can be used interchangeably). Therefore, Onakado '761 reference can be interpreted that it does disclose "applying an erase voltage (fig. 48, -6 to –11V) to the P-type drain region (fig. 48, interchange P-type source 932 with a P-type drain 933), a supply voltage to the control gate (fig. 48, positive potential (+8-+12v)) and said erase voltage (fig. 48, -6 to –11V) to the N-type well region (fig. 48, 931). Also floating the P-type source region (fig. 48, interchange P-type drain 933 with a P-type source 932) (regarding to claim 3).

Claim Rejections - 35 USC ∍ 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is

> most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 9 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

With regard to claim 9, the limitation of "wherein said cell is programmed by applying a **negative supply voltage around –6 to -10** to said P-type drain region" on line 3-4 is not described in the specification. In fact, page 12, line 4 of the specification specifically disclosed that "memory cell is programmed by applying a **negative voltage around –4 to –6 volts** to the drain region to induce hot electron". One can clearly see that the range of –6 to –10 voltage as claimed in the amended claimed is different than the range of –4 to –6 voltage as described in the specification. Nowhere in the specification described or disclosed that the programmed voltage of a negative supply voltage **around –6 to –10** is apply to the P-type drain region.

Claim Rejections - 35 USC ϶ 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1, 3-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Onakado et al, Pat. No. 5818761.

With regard to claim 1, Onakado discloses a non-volatile memory cell structure, said structure comprising: an N-type well region (fig. 51, 1) in a substrate, a channel region (fig. 51, 8) between a P-type source region (fig. 51, 2/3) and a P-type drain region (fig. 51, 3/2), wherein the conductivity type of said P-type is opposite to the conductivity type of said N-type; a first insulator layer (fig. 51, 4) on the surface of said N-type well region (fig. 51, 1); a floating gate (fig. 51, 5) overlying said first insulator layer (fig. 51, 4); a second insulator layer (fig. 51, 6) on said floating gate (fig. 51, 5); and a control gate (fig. 51, 7) on said second insulator layer (fig. 51, 6), wherein said non-volatile memory cell is erased by applying an erase voltage (fig. 51, 5-12V) to said P-type drain region (fig. 51, 3/2, drain and source region are inherently known in the semiconductor art to be interchangeable), a supply voltage (fig. 51, -5 to –12V), and said erase voltage (fig. 51, 5-12V) applied to the N-type well region (fig. 51, 1).

With regard to claim 3, Onakado discloses a source line (fig. 11, SL) couple to said P-type source region (also with regard to claim 6), said source line exhibits floating (fig. 51, element 3/2, note, drain and source are inherently known in the semiconductor art to be interchangeable).

With regard to claim 4, as far as understood, Onakado discloses wherein said source line is divided by an isolation structure along a bit line direction (fig. 11, SL runs parallel is along a bit line SB11-SB01 and MB1-MB0 direction) (also with regard to claim 7).

With regard to claim 5, as far as understood, Onakado discloses a non-volatile memory cell structure, said structure comprising: an N-type well region (fig. 51, 1) in a substrate, a channel region (fig. 51, 8) between a P-type source region (fig. 51, 2/3) and a P-type drain region (fig. 51, 3/2), wherein the conductivity type of said P-type is opposite to said N-type; an insulator layer (fig. 51, 4) overlying said N-type well region (fig. 51, 1); a gate transistor (fig. 51, 7) on said insulator layer; said gate transistor comprise a control gate (fig. 51, 7) coupled to a word line (fig. 11, WL), said P-type drain region (fig. 49A, 3/2) coupled to a bit line (fig. 11, example SB11-SB11); wherein said cell is erased by applying an erase voltage (fig. 51, 5-12V) to said N-well well region, and applying a supply voltage (fig. 51, -5 to –12V) to the control gate (fig. 51, 7).

With regard to claim 8, Onakado discloses wherein said supply voltage (fig. 51, -5 to –12V) to the control gate (fig. 51, 7) is erase voltage (fig. 51, 5-12V).

With regard to claim 9, as far as understood, Onakado discloses wherein said cell is programmed by applying a negative supply voltage around -6- to –10 volts (fig. 49A, -3 to –10V) to said P-type drain region (fig. 49A, 3) to induce hot electrons, and a negative threshold voltage is of about -4 Volts applied to said wordline (fig. 52).

With regard to claim 10, as for as understood, Onakado discloses a method for erasing non-volatile memory cell having a P-type substrate (fig. 10, 20) and an N-type well region (fig. 10, 24) therein, a channel region (fig. 51, 8) between a P-type drain region (fig. 51, 3/2) and a P-type source region (fig. 51, 2/3), said method comprising the steps of: applying an erase voltage (fig. 51, 5-12V) to said P-type drain region (fig. 51, 3/2, drain and source region are inherently known in the semiconductor art to be interchangeable) to cause tunneling oxide layer of electrons from a floating gate to said N-type well region, wherein said P-type drain region (fig. 51, 2/3) coupled to a bit line (fig. 11, SBL and MBL); applying a supply voltage (fig. 51, -5 to –12V) to a control gate (fig. 51, 7), wherein said control gate (fig. 51, 7) coupled to a word line (fig. 11, WL); and grounding said word line of unselected cell and said bit line of unselected cell to cause the P-type drain region as an inhibit switch (col. 21, line 43-45).

Claim Rejections - 35 USC ∋ 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 5-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al, Pat. No. 6671209.

With regard to claim 5, as far as understood, Lin discloses a non-volatile memory cell structure, said structure comprising: an N-type well region (fig. 1, N-well) in a substrate (fig. 1, 10), a channel region (fig. 1, 26) between a P-type source region (fig. 1, 22) and a P-type drain region (fig. 1, 24), wherein the conductivity type of said N-type is opposite to said P-type; an insulator layer (fig. 1, 14) overlying said N-type well region (fig. 1, n-well); a gate transistor (fig. 1,12) on said insulator layer; said gate transistor comprise a control gate (fig. 1, 20) coupled to a word line, said P-type drain region (fig. 1, 24) coupled to a bit line; wherein said cell is erased by applying an erase voltage (fig. 1, Ground) to said N-well well region, and applying a supply voltage (fig. 1, Vg) to the control gate (fig. 1, 20) (col. 2, line 66-col. 3, 13).

With regard to claim 6, Lin discloses a source line couple to said P-type source region (fig. 1, 22), said source line exhibits floating (col. 3, table I) (also with regard to claim 7).

With regard to claim 8, Lin discloses wherein said supply voltage (fig. 1, Vg) to the control gate (fig. 1, 20) is erase voltage (col. 2, line 66-col. 3, 13).

With regard to claim 10, as for as understood, Lin discloses a method for erasing non-volatile memory cell having a P-type substrate (fig. 1, 10) and an N-type well region (fig. 1, n-well) therein, a channel region (fig. 1, 26) between a P-type drain region (fig. 1, 24) and a P-type source region (fig. 1, 22), said method comprising the steps of: applying an erase voltage (fig. 1, Vd) to said P-type drain region (fig. 1, 24) to cause tunneling oxide layer of electrons from a floating gate to said N-type well region, wherein inherently the P-type drain region (fig. 1, 24) coupled to a bit line; applying a supply voltage (fig. 1, Vg) to a control gate (fig. 1, 20), wherein inherently the control gate (fig. 1, 20) coupled to a word line; and grounding said word line of unselected cell and said bit line of unselected cell to cause the P-type drain region as an inhibit switch (col. 3, line 14-col. 4, line 6).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Hsia et al (6747899), Hsu et al (6441443) disclose a memory device having program and erase operation.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP ϶ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached at (571) 272-1787. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to

the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov Should you have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C.Yoha

September 2005

CONNIE C. YOHA
PRIMARY EXAMINER